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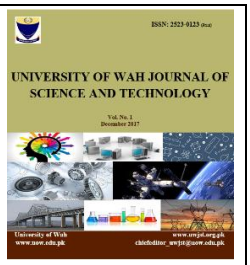

Low-Pass Second-Order Single-bit Delta-Sigma Modulator for Biosensors

A. Hussain

***Abstract*—This paper presents design of a low-pass second-order single-bit Switched-Capacitor (SC) delta-sigma modulator; analog-to-digital converter (ADC) for cascading of integrators with distributed feedforward (CIFF) structure for biosensor applications. The signal transfer function (STF) and the noise transfer function (NTF) of the loop filter of delta-sigma modulator is expressed in terms of poles and zeroes on the unit circle in the z-domain. The NTF zero optimization technique is also implemented to reduce further in-band quantization noise by shaping in-band quantization noise at high frequency. Operational amplifier (op-amp) of the front-end integrator is optimized for minimum power consumption by considering low finite DC-gain, limited slew-rate, minimum required gain-bandwidth product (GBW). The modulator simulations are performed and discussed. Non-ideal effect of the proposed complete CIFF modulator structure for SC circuit level implementation is performed and parameters like thermal noise, op-amp noise, and switch non-linearity is included in the model and results are provided. The op-amp white noise for the front-end integrator is also simulated for different values, including the thermal noise and sampling switch non-linearity. Modeling and simulation result for a CIFF structure with single-bit quantizer, shows that proposed modulator structure can achieve signal-to-noise ratio (SNR) of 89dB for a biosensor system with signal bandwidth of 2kHz having over-sampling ratio (OSR) of 128.**

***Index Terms*— Delta-sigma modulator, Analog-to-digital converter, Switched-Capacitor, Operational amplifier, Integrator**

I. Introduction

THERE is an increase in demand for portable devices that can be utilized for biological signal monitoring. These devices utilizes microelectronics; Micro-Electo-Mechanical-Systems (MEMS) with biomedical signal to improve the health care. These technologies allow portability and ease of use. A biosensor is a sensing device that combines a transducer with the biological sensitive element. There are several types of biosensors classified as enzymatic biosensors, genosensors, immunosensors, etc. They are divided into several different categories based on transduction process, such as electrochemical, optical, piezoelectric, and thermal/calorimetric sensors. One of the most widely used biosensor is electrochemical [1]. The biological signal has a bandwidth of few kHz and dynamic range of about 40dB to 70dB, which is quite relaxing, but the challenge is its power consumption and smaller size due to integration. The ADC is also an important building block of the biosensor required to design with ultra-low power consumption. Wearable electronics for health care are also getting popular due to simple interface and portability. A network of wireless wearable biomedical equipment can provide better treatment; every patient includes biosensor for every node. These biosensors are smart sensor that can get the bio signal and communicate over the network to other nodes. BioMEMS and Bionanotechnology are bio-inspired devices or biochips that are used for delivery, processing, analysis, or detection of biological molecules and species. These types of devices are used to detect cells, microorganisms, viruses, proteins DNA, related nucleic acid, and small molecules of biochemical importance.

A biosensor consists of four steps, first to collect the sample from water, food, air or body fluids. The second step is to do processing or separation. The third step is to detect and convert the signal for further processing. The fourth and final step is to do an analysis of the data. The use of micro and nano-scale detection technologies is justified by reducing the sensor element to the scale of the target species and hence providing a higher sensitivity as its target single entity or molecule. It also reduces the time to obtain results due to small volumes resulting in higher effective concentrations. It

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allows amenability of portability and miniaturization of the entire systems. There are several designs in the literature for the SC design techniques.

Low-voltage, low-power sigma-delta modulator for bio-potential signals performs the measurement of biological signals and has many parallels to the biosensors [2]. A second-order sigma-delta modulator is designed in CMOS 0.18µm technology. The design uses boosted clock voltages to pass signals through switches by using switched op-amp technique. It can achieve signal-to-noise ratio of 70dB for signal bandwidth of 10 kHz [3], [4]. The second design is a low power SC technique utilizing an inverter to develop ADC. This research is intended for audio processing applications but it uses low-power inverter instead of traditional op-amp [5]. The third low-power design uses a single op-amp to achieve high accuracy. A multi-bit digital-to-analog converter (DAC) is used to provide feedback to increase the order of the modulator. The modulator can achieve signal to noise distortion ratio (SNDR) of 84dB over signal bandwidth of 100 kHz with power consumption of 140µW.

The fourth design uses separate analog and digital paths to increase the order of the modulator [6]. The last design uses supply voltage of 250mV to achieve SNDR of 61dB over a 10 kHz bandwidth while consuming 7.5µW [7]. The reduced supply voltage in CMOS technologies for analog signal puts more challenges due to smaller signal swing while the digital design can take advantage of it. It is difficult to reduce the noise floor to enhance the dynamic range. Delta-Sigma Modulator has the key advantage of high linearity with low-bit quantizer and feedback type implementation. It uses the mechanism of oversampling and noise shaping to get high resolution. The front-end of this ADC is analog while the output is completely digital, which is compatible with digital world.

The comparator-based SC Integrator can be designed which is much low-power and efficient than the traditional op-amp [8], [9]. The switched op-amp technique can also be used to reduce the power of the front-end Integrator [10]. An active-passive approach can be very useful to reduce the power of overall modulator by replacing the front-end integrator by GmC integrator. While the second integrator can be replaced by the passive SC integrator to reduce power [11]. The adder in the front of quantizer replaced by adder inside the quantizer as ratio of transistor. The front-end Integrator cannot, be replaced to passive SC integrator as it causes the leakage effect, which degrades the noise shaping performance [12]. A SC technique known as double sampling technique may, also be used to increase the sampling frequency of the modulator [13]. The charge-pump Integrator can replace the front-end Integrator, it has quite small full-scale input while feedback is double then traditional SC op-amp based delta-sigma modulator but even it is low-power alternate [14]. A MOS parametric integrator can also be an alternate to the power hungry traditional op-amp based Integrator for the first Integrator of the proposed modulator [15]. The recommended low-power ADCs in the literature for the biosensors and biomedical application are given as [16-24].

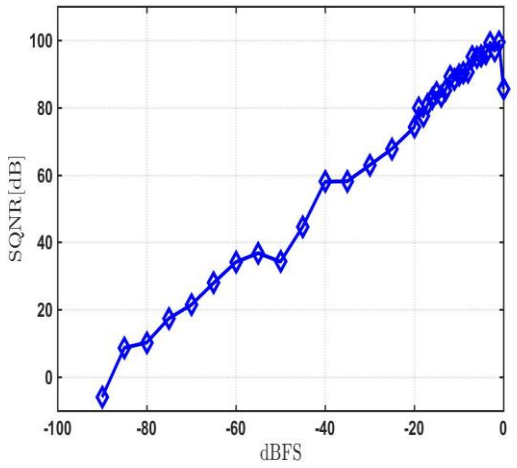

Fig. 1. Dynamic range plot.

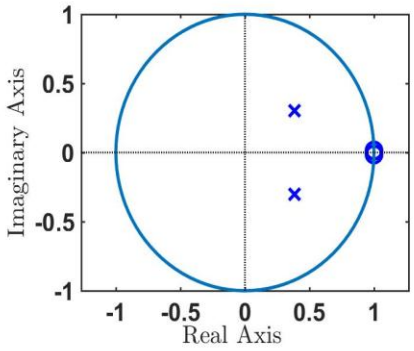

Fig. 2. NTF zero plot on unit circle.

This paper investigates the design of second-order single-bit delta-sigma modulator for a signal bandwidth of 2 kHz using OSR of 128 with minimum power consumption.

II. Delta-Sigma Modulator Design

In this section, the modeling and simulation of CIFF second order single-bit delta-sigma modulator discussed. The second order modulator is selected due to higher stability and moderate dynamic range requirement.

There are several advantages of SC circuit techniques, easily simulated, compatible with VLSI CMOS, insensitive to clock jitter as long as full settling occurs and insensitive to the exact shape of op-amp settling waveform as long as full settling occurs. The pole-zero location is set by capacitor ratio,

TABLE I
CIFF Structure Coefficients

i	a	b	c	g
1	0.8	1	1	0.000101
2	0.4	0	1	0
3	0	1	0	0

which is highly accurate [25], [26], [27]. The low-order single-loop single-bit modulator has the key advantage of guaranteed stability, simple loop filter design, simple SC circuit design, input range may use almost the full range of 1's densities. The single-bit design is easy to implement DAC.

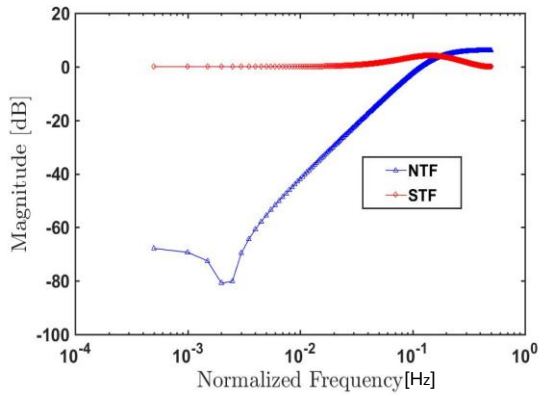

Fig. 3. STF and NTF plot for CIFF.

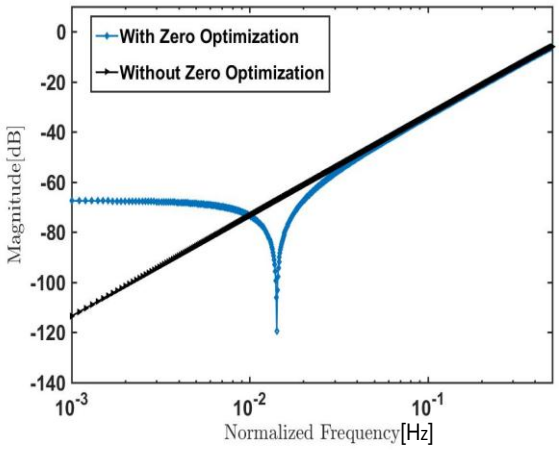

Fig. 4. NTF with and without zero optimization.

CIFF structure with dynamic range for maximum full scale is shown in *Fig. 1*. The signal-to-quantization-noise-ratio (SQNR) versus input signal full scale is plotted. It is shown that modulator can achieve dynamic range more than 90dB. While the modulator can achieve maximum SQNR of 99dB, which is better to keep some margin for SC implementation. *Fig. 2* shows the NTF zeroes and poles plot on the unit circle in the z-domain. It is shown that the zeroes are shifted at DC (Z=1) while the poles are inside the unit circle. Due to the ideal integrator, which used op-amp with infinite gain, the zeroes are in the DC. This causes an ideal second-order noise shaping with roll-off of 20dB/decade.

Fig. 2 also shows clearly that the NTF zero is at DC gain for maximum suppression of quantization noise and effective noise shaping while the poles of the modulator are inside the unit circle. *Fig. 3* shows the STF and NTF plot, as the modulator is low-pass. The STF is flat at low frequencies while the NTF response is high pass to shape the in-band quantization noise at high frequencies, which is later filtered in the digital domain. The STF is flat at low frequencies while NTF shows the high-pass noise shaping. *Fig. 4* shows the NTF plot with or without zero optimization. The straight line shows the actual NTF plot slope without zero optimization, while curve line shows that NTF zero optimization. The zero optimization spread the NTF zero on DC to further enhance the SNR of the modulator, for second order it is about 5dB enhancement. *Fig. 5* shows the block diagram of the CIFF structure second-order single-bit modulator.

III. Simulation Results and Discussion

Fig. 6 shows the transient simulation output and input for two level quantization as output. The output of the modulator is pulse coded modulation (PCM) pattern as represented with the analog input signal. The output power spectral density (PSD) of the modulator is shown in the *Fig. 7.* It shows full-scale input of the modulator is 1.4Vp-p. *Fig. 8* shows the two integrators output states for the CIFF modulator. The output swing of the first Integrator is small while the output swing of

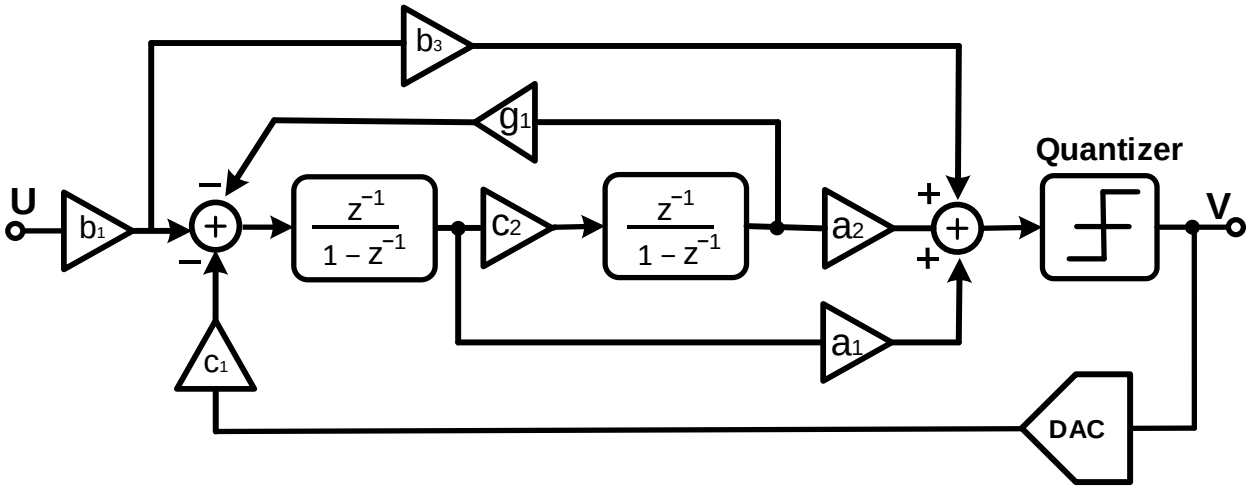

Fig. 5. Block diagram of CIFF structure second-order single-bit modulator.

second Integrator is large. The front-end Integrator is only processing the quantization noise. The swing inside the loop filter is also small which demands low gain op-amp, which is power efficient. In addition, nano-scale CMOS supply voltage is reducing, putting more challenge for the design of high gain op-amp while it is much easier to design low gain op-amp. Table I shows the coefficient for the CIFF modulator for modeling and simulation. Richard Schreier Delta-Sigma Modulator Toolbox is used for modeling [28]. *Fig. 8* shows the Integrator output states for the CIFF structure. First Integrator output swing is small while the second Integrator output swing is large. The key advantage of this structure is single feedback as it is multiple feed forward structure. It also requires one extra adder as op-amp. Due to smaller swing, the first Integrator design is not challenging as it is processing only the quantization noise as the signal is feed forwarded in front of the quantizer. *Fig. 9* shows the general block diagram of the modulator. It consists of two parts, loop filter and quantizer Q. The loop filter is linear and it contains memory elements. The second part is quantizer, which is nonlinear. The loop filter consists of two inputs L_0 = STF/NTF and L_1=1-1/NTF while Y is the output. The output Y can be expressed as a linear combination of input U and feedback signal V. The quantizer is modeled as the addition of quantizer error EQ.

In equation (3), the loop filter L_1 must be large in the signal frequency range 0 to f_B to reduce NTF. In addition, L_0 must be large in the same range to allow STF as unity as shown in equation (4). This means that poles of both L_1 and L_0 are in the same range. While zeroes of L_1 and L_0 will be different as shown in *Fig. 10* [26]. The second-order single-bit modulator with these coefficients is simulated, considering non-ideal effects due to real SC circuit implementation. All these simulations are performed by considering sampling capacitor of 200fF, with non-linear switches and op-amp noise of 10μV/Hz. *Fig. 11* shows the output PSD plot of the modulator.

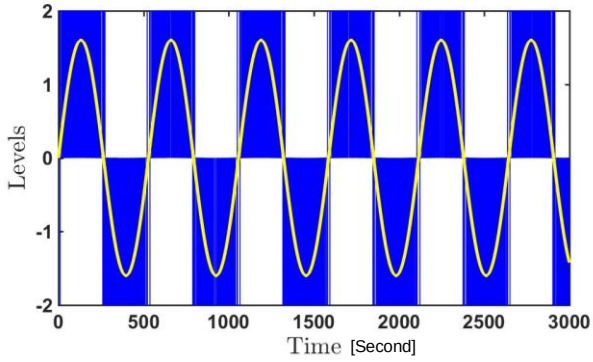

Fig. 6. Transient simulation plot.

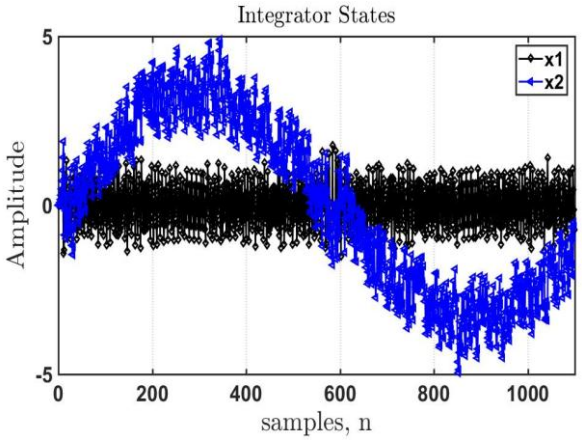

Fig. 8. CIFF Integrator output states.

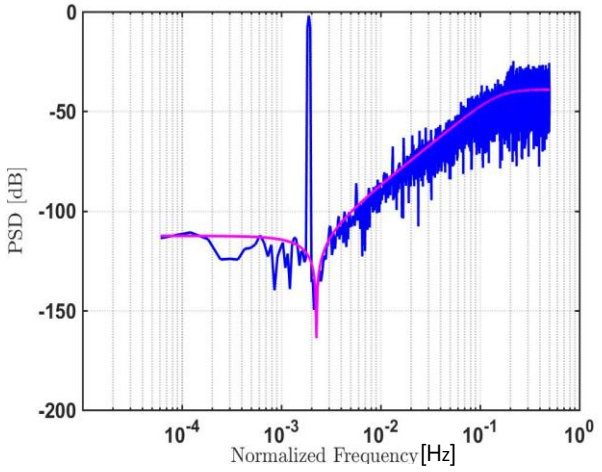

Fig. 7. Output PSD plot.

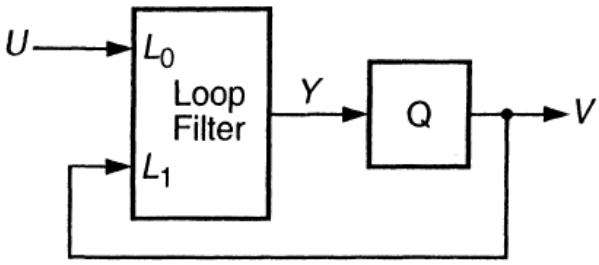

Fig. 9. Single bit quantizer modulator.

$$NTF = \frac{1}{1 - L_1} \tag{1}$$

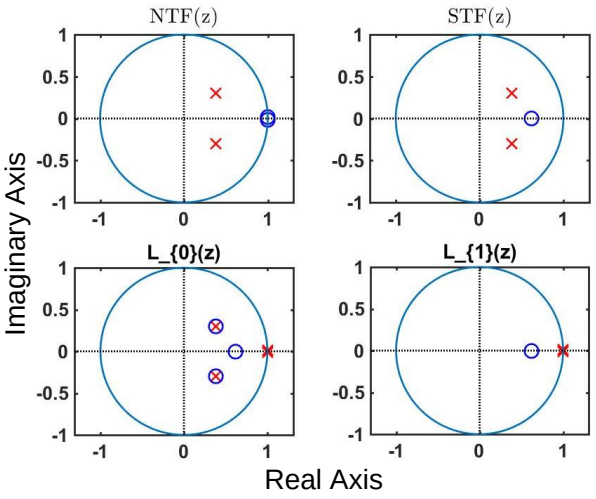

Fig. 10. Loop filter poles and zeroes.

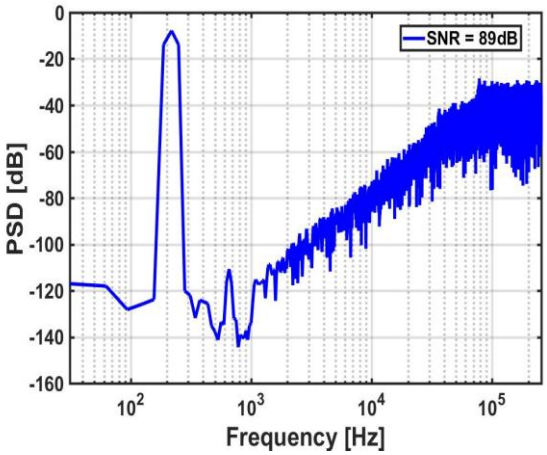

Fig. 11. Output PSD plot.

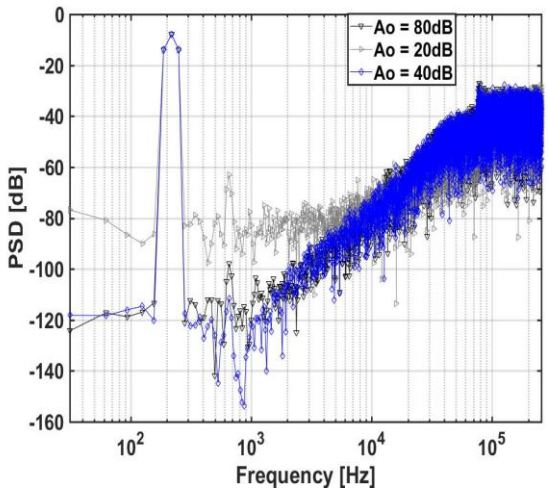

Fig. 12. Op-amp DC gain simulation.

$$NTF = \frac{L_0}{1 - L_1} \tag{2}$$

$$L_1 = 1 - \frac{1}{NTF} \tag{3}$$

$$L_0 = \frac{STF}{NTF} \tag{4}$$

In equation (3), the loop filter L_1 must be large in the signal frequency range 0 to f_B to reduce NTF. In addition, L_0 must be large in the same range to allow STF as unity as shown in equation (4). This means that poles of both L_1 and L_0 are in the same range. While zeroes of L_1 and L_0 will be different as shown in *Fig. 10* [26]. The second-order single-bit modulator with these coefficients is simulated, considering non-ideal effects due to real SC circuit implementation. All these simulations are performed by considering sampling capacitor of 200fF, with non-linear switches and op-amp noise of 10μV/Hz. *Fig. 11* shows the output PSD plot of the modulator. *Fig. 12* shows the Integrator op-amp DC gain simulation results performed in SDToolbox [29], [30]. The reduced op-amp DC gain causes noise shaping degradation; as a result SNR drops. The op-amp DC gain of 80dB is considered for SNR of 91dB. While as the DC gain drop off, the SNR also drops and noise shaping degrades. A detailed simulation results show that with DC gain of 60dB, SNR is 89dB, while DC gain of 40dB resulted SNR of 84dB and DC gain of 20dB resulted SNR of 53dB. Limited slew-rate causes degraded noise shaping performance, hence SNR drops; this effect is illustrated in the *Fig. 13*. *Fig. 14* shows the gain bandwidth (GBW) simulation of the two Integrators and adder in front of the quantizer. The required bandwidth for the Integrators is 1 MHz for SNR of 91 dB. In the case of GBW of 100 kHz, SNR drops to 80 dB while for the case of GBW of 1 kHz, the SNR drops to 62 dB. Due to the two levels of single-bit quantizer, there is no mismatch issue of the front-end Integrator of the modulator. It shows that the front-end DAC is important and mismatch does not cause performance degradation.

The circuit level implementation has many non-ideal effects like thermal noise kT/C, op-amp noise and front-end sampling switches nonlinearity [27]. To suppress the non-ideal effects, typically large capacitor is required, hence more power hungry op-amp is needed to drive these large capacitors. The white noise known as op-amp noise effect is also simulated as shown in the *Fig. 15*. Simulations show that higher op-amp noise sets higher noise floor level in the output PSD, which degrades the SNR of the modulator. The lower op-amp noise gives power-efficient op-amp design. The front-end Integrator requires special consideration to suppress the circuit non-idealities. Inverter based design can be used to design front-end integrator, to reduce the power of the proposed modulator [5]. The adder in front of quantizer needs to be replaced by a passive adder or built-in adder in the quantizer that already exists in the literature.

IV. CONCLUSIONS

This paper discusses the modeling and simulation of second-order single-bit delta-sigma modulator ADC design for biosensors application. Simulation results show that proposed modulator structure can achieve SNR of 99dB ideally. Due to CIFF structure selection, the signal swing inside the loop filter will be smaller. The op-amp does not demand large DC gain as it is much easier to design. It shows that the modulator can achieve SNR of 89dB by considering thermal noise, sampling switch nonlinearity and op-amp noise. The op-amp DC gain, slew-rate and GBW are also simulated and results are presented to estimate the performance degradation at the circuit level implementation. The effect of the op-amp noise is also simulated by considering all the other non-idealities.

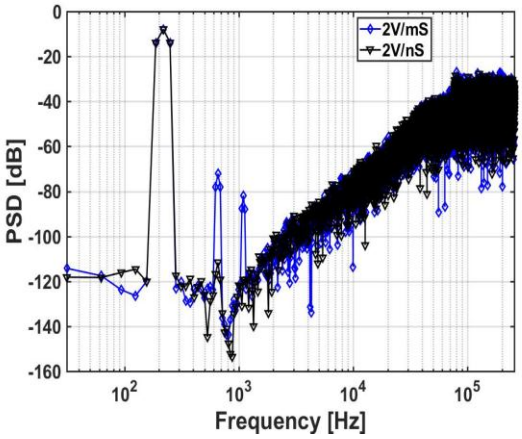

Fig. 13. Slew-rate simulation.

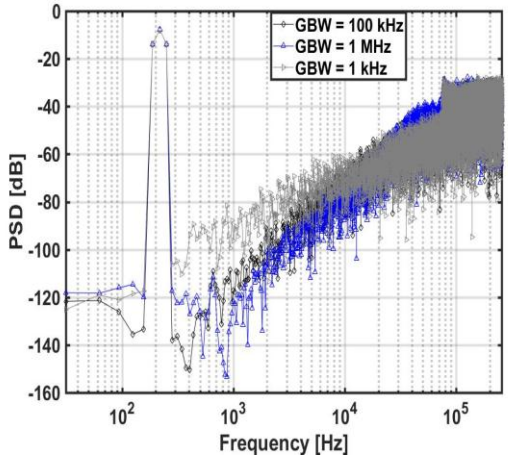

Fig. 14. GBW simulation.

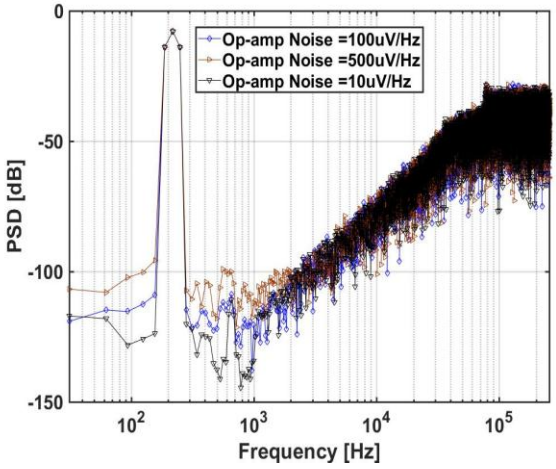

Fig. 15.Opamp noise simulation.

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